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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|--|-------------|----------------------|---------------------|------------------|
| 10/646,013 | 08/22/2003 | Cheng H. Huang | A1063 | 8979 |
| 36532 | 7590 | 07/26/2004 | EXAMINER | |
| G. VICTOR TREYZ FLOOD BUILDING 870 MARKET STREET, SUITE 984 SAN FRANCISCO, CA 94102 | | | FORDE, REMMON R | |
| | | | ART UNIT | PAPER NUMBER |
| | | | 2826 | |

DATE MAILED: 07/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

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|------------------------------|--------------------------------------|-------------------------------------|--|
| Office Action Summary | Application No. 10/646,013 | Applicant(s) HUANG ET AL. | |
| | Examiner Remmon R. Fordé | Art Unit 2826 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 August 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) 19-23 is/are withdrawn from consideration.
- 5) ☒ Claim(s) 10-18 is/are allowed.
- 6) ☒ Claim(s) 1-4, 6 and 9 is/are rejected.
- 7) ☒ Claim(s) 5, 7 and 8 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>8/18/2004</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response To Election

Examiner hereby acknowledges Applicant's election of claims 1-18, without traverse, in correspondence dated 08/16/2004.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4, 6 and 9 are rejected under 35 U.S.C. 102(e) as being anticipated by Novosel et al..

Regarding claims 1, 4 and 9, referencing Figures 1A-5B, Novosel et al. discloses an electrically-programmed integrated circuit antifuse circuitry formed from a semiconductor provided with a MOS transistor antifuse (M1) having a drain (308), source (306) gate (302), and substrate (310), wherein the drain and substrate form a drain-substrate p-n junction in the semiconductor; and circuitry connected to the antifuse transistor that applies a voltage to the drain that causes avalanche breakdown

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of the drain-substrate p-n junction and a rise in voltage at the substrate that turn the antifuse transistor on and produces sufficient current between the drain and source to melt the semiconductor and program the antifuse. (Page 2, Paragraph [0020] – Page 6, Paragraph [0048].)

Regarding claim 2, referencing Figure 3A, Novosel et al. further discloses that the gate (302) has only a polysilicon layer. (Page 4, Paragraph [0030].)

Regarding claim 3, referencing Figures 2 and 3A, Novosel et al. further discloses providing sensing circuitry that senses whether the antifuse transistor has been programmed and outputs a high or low logic signal accordingly. (Page 4, Paragraph [0030].)

Regarding claim 6, referencing Figures 2 and 3A, Novosel et al. further discloses providing a metal that electrically interconnects the gate and the source. (Page 4, Paragraph [0030].)

Allowable Subject Matter

Claims 5, 7 and 8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 10-18 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

Claim 10 recites an electrically-programmable integrated circuit antifuse circuitry structure including the specific structural limitations of providing at least one Zener diode connected between the drain and the substrate; and circuitry connected to the antifuse transistor and Zener diode that applies a voltage to the drain which causes Zener breakdown of the Zener diode and a rise in voltage at the substrate that turns the antifuse transistor on and produces sufficient current between the drain and source to melt the semiconductor and program the antifuse. The abovementioned structural limitations are neither anticipated by nor obvious over the prior art of record. Likewise, claims 11-18 are also allowable as being dependent upon allowable claim 10.

Relevant Prior Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kim et al., Kowalski, Yang et al., Au et al. and Forbes each disclose MOS transistor antifuse devices.

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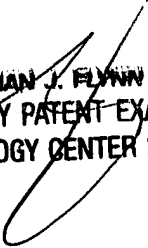
Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Remmon R. Fordé whose telephone number is (571) 272-1916. The examiner can normally be reached on Monday-Thursday (8:00-6:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Remmon R. Fordé


NATHAN J. FLYNN
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